Single Event Effects Characterization of Dosed UT200SpWPHY01 SpaceWire Physical Layer Transceiver

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***Abstract*—We present SEE test results for the Cobham SpaceWire transceiver after dosing the device to 300 krad(Si). We performed SEU characterization with variable data rates and patterns. Events resembling SEFIs were also observed and recorded.**

I. Introduction

SPACEWIRE is a standardized spacecraft data handling and communication network based on the IEEE 1335 standard; it is simple to implement, relatively high speed, low power, and robust [1]. Therefore, it has been adopted and widely used by ESA, NASA, and JAXA for many significant missions. Cobham's UT200SpWPHY01 PHY transceiver is designed to handle the critical timing issues associated with the SpaceWire data and strobe encoding method and eliminate the use of standalone Low-Voltage Differential Signaling (LVDS) drivers and receivers. This chip is manufactured on a 250 nm logic EPI silicide silicon Complementary Metal-Oxide Semiconductor (CMOS) process at a TSMC foundry. According to Cobham, this device has been successfully tested up to 100 krad(Si) total dose per MIL-STD-883 Method 1019 and has proven to be immune to latch-up at high Linear Energy Transfer (LET), (LET > 109 MeV-cm^2/mg) [2].

This data workshop presents complete heavy ion induced Single Event Upset (SEU) characterization data for the SpaceWire PHY transceiver (UT200SpWPHY01). The SEU cross-section for this device is small based on Cobham's SEE qualification report [3]. They reported a saturated cross-section of about 1E-7 cm^2 and LET threshold of 38 MeV-cm^2/mg. Additionally, they described seeing events resembling Single Event Functional Interrupts (SEFIs) where bursts of multiple bit-errors occurred. The main differences between our test and Cobham's are the data transmission rate and pattern, the wider range of heavy ions used, greater beam fluence, and the fact that our parts were pre-dosed to 300 krad(Si) for harsh radiation environment mission compatibility. They tested at a constant, low transmission rate of 24 Mbps while we tested at 240, 200, and 50 Mbps, which resulted in lowering the LET threshold, increasing the SEU cross-section, and recording numerous "burst" events or SEFIs.

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II. Experimental Procedure

A. Device Features

The device features include 2-bit Serializer/Deserializer (SerDes) functionality, transmit and receive rates of 200 Mbps or more, 3.3V supply voltage (V_{DD}), radiation-hardened design, and 28-pin flatpack ceramic package. All control, clock, and single ended data signals to the device are 3.3V Low-Voltage CMOS (LVCMOS) input/output type while all transceiver signals are low voltage differential signaling (LVDS) pairs [2]. The device block diagram is shown in Figure 1.

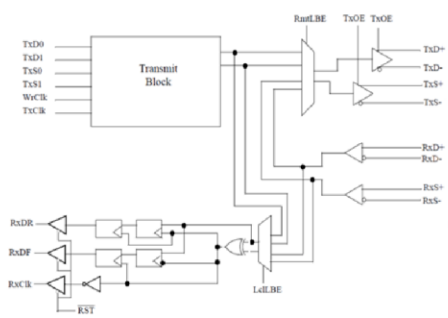

Figure 1. UT200SpW PHY Chip Block Diagram

B. Test Samples

Two test samples were irradiated to 300 krad(Si) in the Cobalt-60, high dose rate cell at JPL with a 20 rad(Si)/s dose rate. The samples were dosed approximately a week before the SEE test. Supply currents for both devices were measured and recorded for pre and post irradiation; functional tests were also performed. Our test samples consisted of 1 biased, 1 unbiased condition parts, and 2 virgin parts for control. The test samples are shown in Table I.

Table I. UT200SpWPHY01 300 krad(Si) Dosed SEE Test Samples

SN	TID Test Condition	Date Code	TID Level krad(Si)
4401	biased (3.6V)	1718	300
4406	unbiased (Ground)	1718	300

The biased condition is shown in Figure 2. For the unbiased condition, we grounded all pins, irradiating the device without supplying power to V_{DD} and not driving any of the input/output signals.

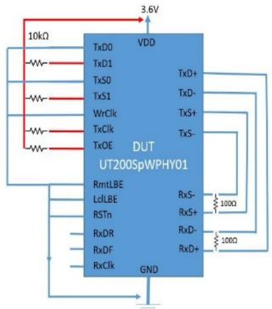

Figure 2. Device Biased Condition for TID Test

C. *Test Parameters and Facility*

We closely followed Cobham's SEE qualification report for the DUT. For the heavy ion induced SEE characterization, we used Texas A&M University's (TAMU) K500 Cyclotron [4]. Ions used for the test are listed in Table II. Furthermore, we tested for worst-case SEU test conditions by setting the supply voltage (V_{DD}) to 3.0V and running at 20°C ambient temperature. We varied our beam flux from 5e4 up to 3e5 $cm^{-2}s^{-1}$ and tested to effective fluence of 1e7 to 1e8 cm^{-2} per run while doing a LET sweep at 15 MeV beam energy. All test runs were done at zero degree angle of incidence. For Krypton (Kr), we used degraders to increase the LET to 33 MeV-cm^2/mg.

Table II. List of Heavy Ions Used for our SEU Test at TAMU

Ion	Beam (MeV)	LET (MeV-cm^2/mg)	Range (um)
Cu	15	19.6	142
Kr	15	27.8	134
Ag	15	42.2	119.3
Xe	15	51.5	119.7
Pr	15	58.3	117.5
Ho	15	75	74.1

D. *Test Setup*

In order to perform the bit-error rate test on the SpaceWire transceiver, we used one of our general SEE test setups. It includes a Xilinx Virtex 4 FPGA evaluation board and our in-house designed and fabricated Device Under Test (DUT) card shown in Figure 3. The system block diagram is shown in Figure 4 and the actual test setup in front of the TAMU K500 beam line is shown in Figure 5.

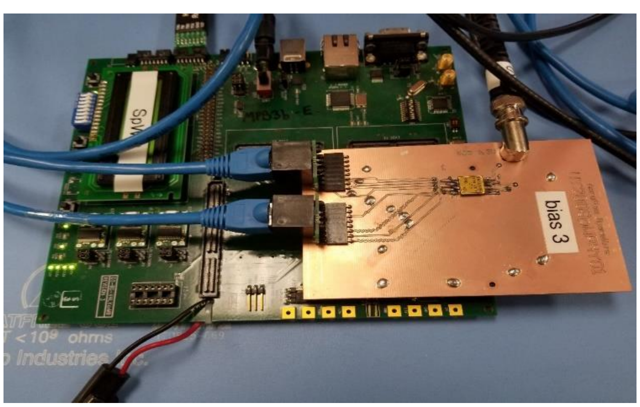

Figure 3. Xilinx V4 Evaluation Board with the DUT on our Custom Daughter Card

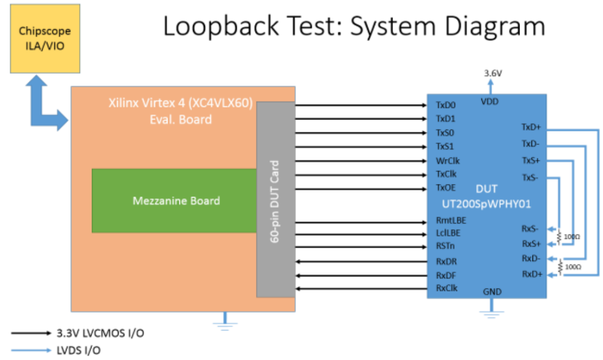

Figure 4. Transceiver Loopback Test Diagram

The FPGA firmware was written in Verilog using Xilinx ISE Design Suite 14.7 for synthesis, place and route, and generating the bit files. Xilinx Chipscope Integrated Logic Analyzer (ILA) and Virtual Input/Output (VIO) were used as the front-end interface for controlling and monitoring the data transfer and error rate. The DUT cards were designed and fabricated with all LVDS constraints in mind. For the functional test, we performed a half-duplex, loopback data transmission over a 6 feet Ethernet cable while transmitting the following raw-data patterns: all 0s, all 1s, 0xCC (11001100), and Linear-Feedback Shift Register (LFSR) pseudo-random. Additionally, we varied the data transmission rate between 240, 200, and 50 Mbps. The device supply voltage and current were monitored and logged during all test runs.

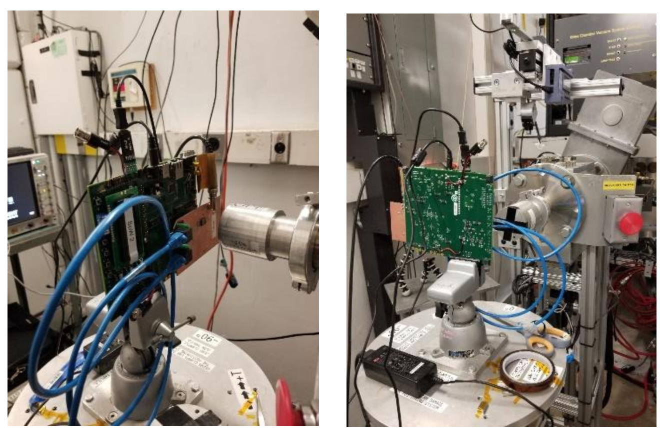

Figure 5. Loopback Test Setup in Front of the TAMU Heavy Ion Beam

III. Test Results and Discussion

We characterized two devices for SEU. Both devices were dosed to 300 krad(Si) before being exposed to heavy ions. We did not observe any bit errors for the all 0 data pattern transmission up to a LET of 75 MeV-cm^2/mg. There was slight frequency dependency for the SEU cross-section. We tested at 50, 200, and 240 Mbps and observed a minor increase in the cross-section, seems to be linear, and fall well within the error-bars. The most comprehensive data was collected at 200 Mbps and pseudo random pattern test parameters; this will be used for future-mission rate calculation. More importantly, we observed two types of bit errors (single and burst) as previously verified by Cobham in [2]. A "single" bit error event can be described as a generic single bit flip/upset that causes the bit error counter in our FPGA firmware to increment by 1. It does not require a hard reset (resets the PHY chip and the FPGA data transmission), and it is most likely a common flip-flop or latch upset. The "single" SEU versus LET cross-sections for both devices are shown in Fig. 6 and 7.

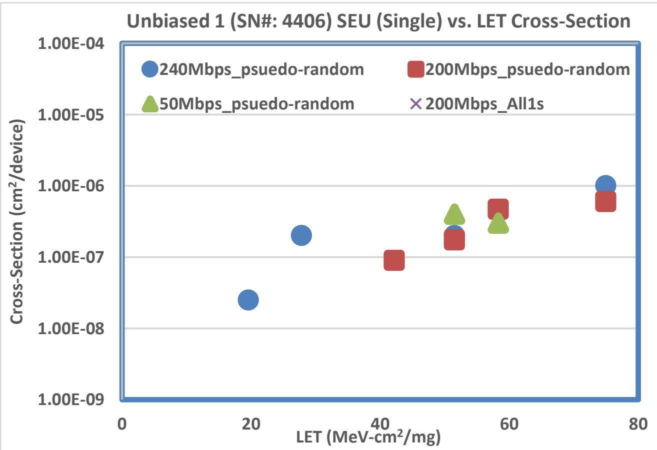

Figure 6. Unbiased Device "Single" SEU Cross-Section as a Function of LET

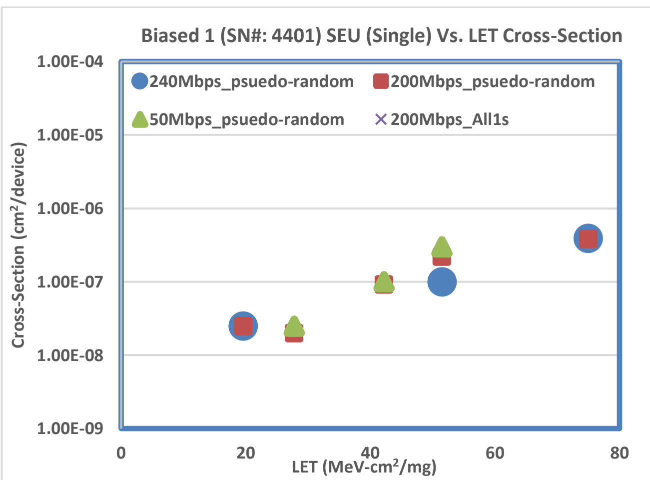

Figure 7. Biased Device "Single" SEU Cross-Section as a Function of LET

The "burst" bit-errors/events that we detected can be split into two categories. In the first case, the bit-error counter increments or jumps by a random number generally in the range of two to a few thousands bit errors and the data transmission continues without further errors or the need to initiate a reset. For the second case, the counter increments uncontrollably and does not recover on its own. This bit-error runaway case requires a reset before continuing with the test; this case can be considered as a SEFI [5]. This event is most likely caused by an upset to the recovered clock (RxClk) path of the DUT which could result in a missed clock edge that could further cause misalignment between the receive data and clock going to the FPGA. The "burst" SEU versus LET cross-sections for both devices are shown in Fig. 8 and 9.

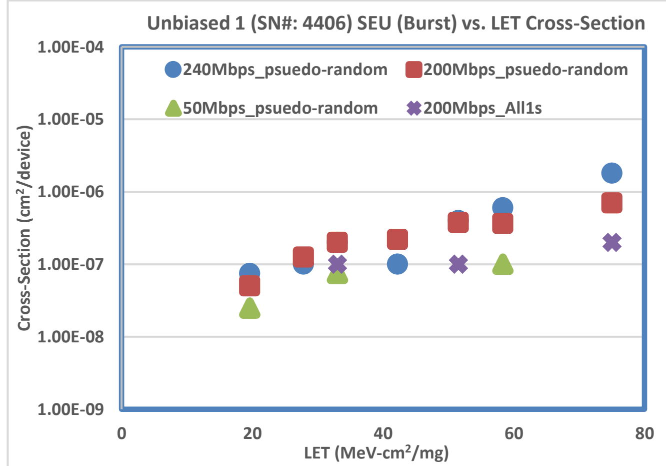

Figure 8. Unbiased Device "Burst" SEU Cross-Section as a Function of LET

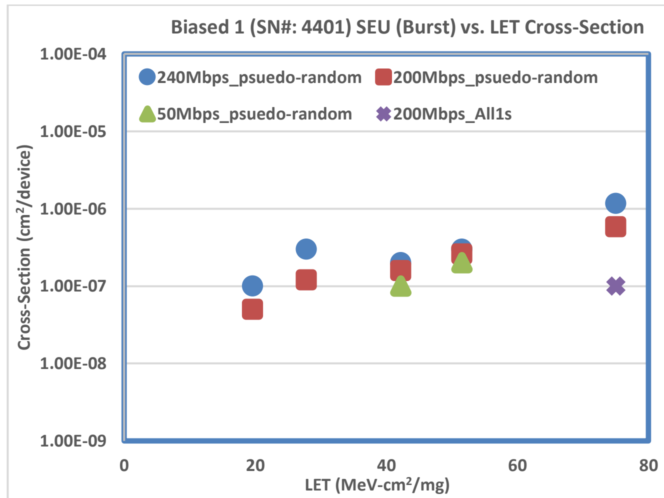

Figure 9. Biased Device "Burst" SEU Cross-Section as a Function of LET

Although the failure or error profile of the burst events is more like SEFIs than SEUs, we categorized each burst event as a SEU (Cobham used a similar approach in their report). We call these combined SEUs "Total" cross-sections, which are shown in Fig. 10 and 11. This not only helps us calculate a more accurate rate; it also allows us to remove any confusion or questions since the device mechanism for the cause of the burst event is unknown and somewhat unpredictable. Furthermore, it is our understanding that the SpaceWire protocol can be interrupted (dropped link) by even a single bit error in a packet during transmission, which requires re-instantiating the link and restarting data transmission. It is highly recommended to perform device reset every time the link is dropped or a bit error is detected. "Burst" events were reported as rare events in Cobham's SEE report. However, for our SEU cross-sections, burst events are for the most part the dominant events and the reason behind the bigger SEU cross-section. The sudden increase in the number of burst events/SEFIs is directly correlated with the faster clock/data rate we operated our test setup compared to Cobham's 24 MHz. At higher clock rates, it is much more likely to observe clock and data transients. The SEU test results are listed in Table III.

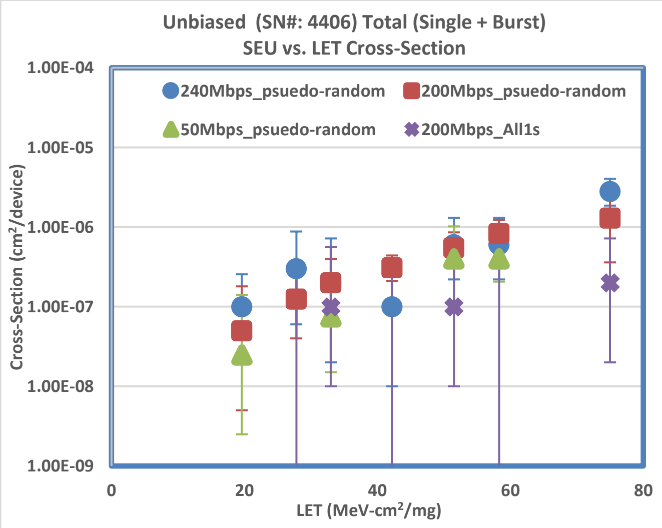

Figure 10. Unbiased Device "Total" SEU Cross-Section as a Function of LET

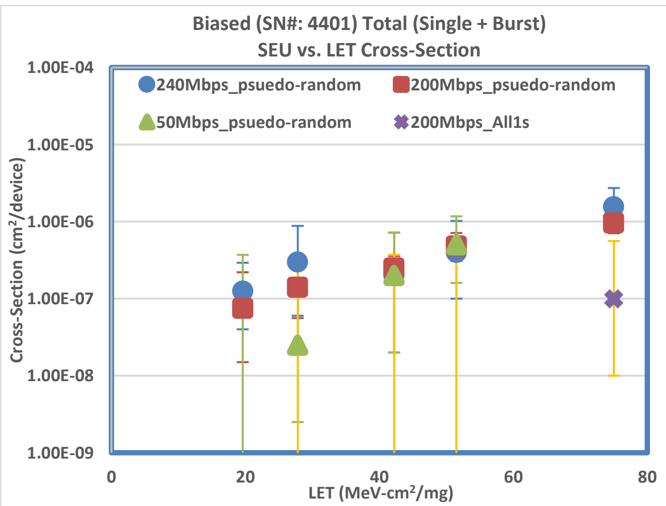

Figure 11. Biased Device "Total" SEU Cross-Section as a Function of LET

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Table III. Summary of SEU Test Results

Device	SEU Threshold (MeV-cm^2/mg)	SEU Saturation Cross-Section (cm^2/device)
UT200SpWPHY	< 19.6	$1x10^{-6}$

IV. Conclusion

The SEU cross-section in general for this device is small based on both Cobham's and our SEE test results. While the single bit error cross-section is slightly frequency dependent, the SEFI or burst event cross-section is highly dependent on the transmission rate (clock speed). Based on our results, the 300 krad(Si) total dose did not have any significant effect on our results as expected for a simple, rad-hard CMOS technology device. Also, there were certainly no distinguishable difference between the two samples. For SEE rate calculation, it is highly recommended to use the data from the "Total" SEU cross-section.

References

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[5] M. D. Berg, "Example 1: Trading ASIC and FPGA considerations for system insertion," presented at the IEEE Nuclear and Space Radiation Effects Conf. Short Course, 2009.